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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/856,613	05/24/2001	Jean-Marc Dery	2202/50001	9727

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EXAMINER	
GELAGAY, SHEWAYE	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 12/15/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/856,613	DERY ET AL.	
	Examiner	Art Unit	
	Shewaye Gelagay	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/24/01*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 have been examined.

Specification

2. The disclosure is objected to because of the following informalities: On page 7, line 11 "a random-access memory" should have been "programmable read-only-memory" as explained on Figure 2. Appropriate correction is required.

Claim Objections

3. The numbering of claims is not in accordance with 37 CFR 1.126 which requires the original numbering of the claims to be preserved throughout the prosecution. When claims are canceled, the remaining claims must not be renumbered. When new claims are presented, they must be numbered consecutively beginning with the number next following the highest numbered claims previously presented (whether entered or not).

Misnumbered claims 20-21have been renumbered 19-20.

4. Claims 20 and 21 are objected to because of the following informalities: They are labeled as amended they should have been labeled as new. Appropriate correction is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-3, 6-8, 11 and 16 are rejected under 35 U.S.C. 102(e) as being anticipated by Segars et al. United States Letter Patent Number 6,052,774.

As per claim 1:

Segars et al. teach a method of protecting data in a system including a microprocessor (106) (Figure 1, item 100) having at least one hardware break point (301), (Col. 8, lines 40-41; embedded ICE unit contains two hardware breakpoint units) characterized in that it includes an operation of allocating a break point to data to be protected, in that it consists of instigating in said microprocessor (106) the generation of a break or interrupt (301) each time one of said protected data is accessed. (Col. 8, lines 42-44; Col. 8, lines 51-52)

As per claim 2:

Segars et al. teach a method characterized in that it includes an access validity verification operation (302, 303) each break (301) triggered by hardware break point allocated to protected data. (Col. 8, lines 53-56; comparator matches the attributes of the breakpoint registers with corresponding attributes contained in the information about data accesses)

As per claim 3 and 11:

Segars et al. teach a method characterized in that it includes an operation (302) of verifying the programming of the control registers at each break (301) triggered by a

hardware break point allocated to protected data. (Col. 10, lines 3-7; a number of additional fields are added to the control registers, each field corresponding to a particular exception routine, and each field being settable to indicate that the debugger wishes to identify an access to the corresponding routine; **adding a number of additional fields to the control registers** reads on **programming of the control registers**)

As per claim 6:

Segars et al. teach a device for protecting data in a system including a microprocessor (106) (Figure 1, item 100) having at least one hardware break point, (Col. 8, lines 40-41; embedded ICE unit contains two hardware breakpoint units) characterized in that it includes means (106) for allocating a break point to data to be protected. (Col. 8, lines 42-44; Col. 8, lines 51-52)

As per claim 7:

Segars et al. teach a device characterized in that it includes means (106) for verifying the validity of each access corresponding to a break triggered by a hardware break point allocated protected data. (Col. 8, lines 53-56; comparator matches the attributes of the breakpoint registers with corresponding attributes contained in the information about data accesses)

As per claim 8 and 16:

Segars et al. teach a device characterized in that it includes means (106) for verifying the programming of the control registers. (Col. 10, lines 3-7; a number of additional fields are added to the control registers, each field corresponding to a

particular exception routine, and each field being settable to indicate that the debugger wishes to identify an access to the corresponding routine; **adding a number of additional fields to the control registers** reads on **programming of the control registers**)

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

8. Claims 4, 12-13, 9 and 17-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Segars et al. United States Letter Patent Number 6,052,774 in view of Sakaki EP 0 735 488.

As per claims 4, 12 and 13:

Segars et al. teach all the subject matter as described above. Not explicitly disclosed by Segars et al, is that a method characterized in that it includes an operation (303) of verifying that the interrupt return address is in the authorized area of the program at each break (301) triggered by a hardware break point allocated to protected data.

Sakaki in analogous art, however, discloses an address sensing means for comparing the address set at the program area setting means with an address being accessed by the program currently being executed to sense whether it is an enable address or a disable address. (Col. 3, lines 3-6)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Segars et al. to include a method characterized in that it includes an operation (303) of verifying that the interrupt return address is in the authorized area of the program at each break (301) triggered by a hardware break point allocated to protected data. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so as suggested Sakaki, (Col. 2, lines 18-19) in order to increase the security of the programs and the data. This way, the address sensing means will verify whether the return address is in the authorized area or not.

As per claim 9, 17 and 18:

Segars et al. teach all the subject matter as described above. Not explicitly disclosed by Segars et al, is that a device characterized in that includes means (106) for verifying that the interrupt return address is in the authorized area of the program.

Sakaki in analogous art, however, discloses an address sensing means for comparing the address set at the program area setting means with an address being accessed by the program currently being executed to sense whether it is an enable address or a disable address. (Col. 3, lines 3-6)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Segars et al. to include a method characterized in that it includes an operation (303) of verifying that the interrupt return address is in the authorized area of the program at each break (301) triggered by a hardware break point allocated to protected data. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so as suggested Sakaki, (Col. 2, lines 18-19) in order to increase the security of the programs and the data. This way, the address sensing means will verify whether the return address is in the authorized area or not.

9. Claims 5,10, 14 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Segars et al. United States Letter Patent Number 6,052,774 in view of Kodama et al. United States Letter Patent Number 5,983,349.

As per claim 5 and 14:

Segars et al. teach all the subject matter as described above. Not explicitly disclosed by Segars et al. is a method characterized in that it includes an operation (305) of invoking an error manager if at least one verification operation (302, 303) gives a negative result.

Kodama et al. in analogous art, however, disclose a method where if the password numbers are found not to coincide with each other the execution of the command is rejected and an error signal is sent. (Col. 9, lines 8-10)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Segars et al. to include a method characterized in that it includes an operation (305) of invoking an error manager if at least one verification operation (302, 303) gives a negative result. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so as suggested Kodama et al., in order to adequately protect the security data in the system. (Col. 1, lines 51-52). This way, if verification is failed at any of the steps disclosed above, protected data will not be accessed.

As per claim 10 and 19:

Segars et al. teach all the subject matter as described above. Not explicitly disclosed by Segars et al. is a device characterized in that it includes means (106) for invoking an error manager if at least one verification means supplies a negative verification result.

Kodama et al. in analogous art, however, disclose a device if the password numbers are found not to coincide with each other the execution of the command is rejected and an error signal is sent. (Col. 9, lines 8-10)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Segars et al. to include a device characterized in that it includes means (106) for invoking an error

manager if at least one verification means supplies a negative verification result. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so as suggested Kodama et al., in order to adequately protect the security data in the system. (Col. 1, lines 51-52). This way, if verification is failed at any of the steps disclosed above, protected data will not be accessed.

10. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Segars et al. United States Letter Patent Number 6,052,774 in view of Sakaki EP0735488 and further in view of Kodama et al. United States Letter Patent Number 5,983,349.

As per claim 15:

Segars et al. and Sakaki teach all the subject matter as described above. Neither of the references explicitly teach a method characterized in that it includes an operation (305) of invoking an error manager if at least one verification operation (302, 303) gives a negative result.

Kodama et al. in analogous art, however, disclose a method where if the password numbers are found not to coincide with each other the execution of the command is rejected and an error signal is sent. (Col. 9, lines 8-10)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Segars et al. and Sakaki to include a method characterized in that it includes an operation (305) of invoking an error manager if at least one verification operation (302, 303) gives a negative result. This modification would have been obvious because a person having

ordinary skill in the art would have been motivated to do so as suggested Kodama et al., in order to adequately protect the security data in the system. (Col. 1, lines 51-52). This way, if verification is failed at any of the steps disclosed above, protected data will not be accessed.

As per claim 20:

Segars et al. and Sakaki teach all the subject matter as described above. Neither of the references explicitly teach a device characterized in that it includes means (106) for invoking an error manager if at least one verification means supplies a negative verification result.

Kodama et al. in analogous art, however, disclose a device if the password numbers are found not to coincide with each other the execution of the command is rejected and an error signal is sent. (Col. 9, lines 8-10)

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the method disclosed by Segars et al. and Sakaki to include a device characterized in that it includes means (106) for invoking an error manager if at least one verification means supplies a negative verification result. This modification would have been obvious because a person having ordinary skill in the art would have been motivated to do so as suggested Kodama et al., in order to adequately protect the security data in the system. (Col. 1, lines 51-52). This way, if verification is failed at any of the steps disclosed above, protected data will not be accessed.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shewaye Gelagay whose telephone number is 571-272-4219. The examiner can normally be reached on 8:00 am to 5:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Shewaye Gelagay
Examiner
Art Unit 2133

11/26/04

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